Spring 2018

ESE 218: Digital Systems Design

Instructor: Dmitri Donetski
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Office Hours: Tuesday, Thursday, 3-5 PM, room 247 Light Eng. bldg.

Prerequisites: Engineering Major: PHY 127 or 132 or 142, or ESE 124; Computer Science Major: CSE 220

Description: The course covers binary numbers, Boolean algebra, arithmetic circuits, flip-flops, analysis and design of sequential circuits, memory and programmable logic. Circuits are designed and simulated in Active-HDL (Aldec), assembled on a breadboard and verified/debugged with a pattern generator/logic analyzer.

Goal: Learning basic theory and development of practical skills for taking next level ECE courses.

Outcomes: students will develop 1) understanding fundamentals of analysis and design of standard building blocks and systems; 2) skills in reading schematic of digital circuits and analysis of circuit behavior; 3) skills in design of combination and sequential circuits using conventional methods and CAD tools; 4) skills in verification and troubleshooting circuits with the pattern generator and logic analyzers, determination of signal propagation delays.

Lectures: 101 Javitz, Tuesday, Thursday, 5:30-6:50 PM

Labs: Room 235 Heavy Eng. bldg (new addition). Lab attendance (experiments) start from the 3rd week.
Section 1, Monday, 12:55-3:55 PM
Section 2, Monday, 7:00-10:00 PM
Section 3, Tuesday, 7:00-10:00 PM

Textbook (required): M. Morris Mano, Michael D. Ciletti, "Digital Design", Pearson, 6th or 5th edition. 6th ed: 2017, ISBN-13: 978-0470531082, ISBN-10: 0470531088, 5th ed.: 2013, ISBN-13: 978-0-13-277420-8, ISBN10: 013-277420-8. All homeworks, prelab and lab assignments with instructions will be posted on the Blackboard.

Laptop: A laptop operating under Windows is required for simulation assignments (prelabs).

Prelab reports are due by midnight before the lab session (submitted by e-mail). Final lab reports are due at the beginning of the next week lab session. Final lab reports have to be printed.

Grading: Lab reports (33 %), Homeworks (11 %), Test 1 (10 %), Test 2 (15 %), Final exam (25 %), Portfolio (6 %)

For passing the course all prelab reports (simulations) from individual students and all final lab reports from a team of 2 students have to be submitted, attendance of all lab sessions is required.

Topical outline:

Binary numbers and codes: 5 % Boolean algebra, logic transformation and minimization: 20 % Arithmetic circuits, decoders, multiplexers, latches and flip-flops: 25 %. Analysis and design of sequential circuits: 30 % Memory and programmable logic: 20 %

References:

1. F. Vahid, Digital Design with RTL Design, VHDL, and Verilog, 2nd ed, 2010, ISBN-13: 978-0470531082, ISBN-10: 0470531088
2. D.M. Harris, S.L. Harris, Digital Design and Computer Architecture, 2nd ed., 2012, ISBN-13: 978-0123944245, ISBN-10: 0123944244
3. J. Wakerly, Digital Design: principles and practices, with Verilog, 5th ed., 2017, ISBN-13: 978-0134460093, ISBN-10: 013446009X
4. W. Kleitz, Digital Electronics: A Practical Approach with VHDL, 9th ed, 2011, ISBN-13: 978-0132543033, ISBN-10: 0132543036