Fall 2019

ESE 118: Digital Logic Design

Instructor: Dmitri Donetski

E-mail: dmitri.donetski@stonybrook.edu

Office Hours: Wednesday, Friday, 3-5 PM, room 247 Light Eng. bldg.

Prerequisites: Engineering Major: ESE 123; Computer Science Major: CSE 220

Description: The course covers binary numbers, Boolean algebra, arithmetic circuits, flip-flops, analysis and design of sequential circuits, memory and programmable logic. The circuits are designed and simulated with CAD tools, assembled on breadboards and verified with the digital pattern generator and the logic analyzer.

Goal: Development of general background in theory and practical skills necessary for taking advanced courses.

Outcomes: students will develop 1) understanding fundamentals of analysis and design of digital circuits and standard building blocks; 2) skills in reading schematic of digital circuits and analysis of circuit behavior; 3) skills in design of combination and sequential circuits using conventional methods and CAD tools; 4) skills in verification and troubleshooting circuits with pattern generators and logic analyzers, determination of signal propagation delays.

Lectures: Lecture hall 102, Light Eng. bldg., Monday, Friday, 1:00-2:20 PM

Labs: Room 235 Heavy Eng. bldg (new addition): the lab experiments start from the 3rd week.
Section 1, Monday, 3:55-6:55 PM
Section 3, Tuesday, 7:00-10:00 PM
Section 4, Wednesday, 7:00-10:00 PM

Requirements: 1) Textbook: M. Morris Mano, Michael D. Ciletti, "Digital Design", Pearson, 6th or 5th edition. 6th ed: 2018, ISBN-10: 0134549899, 0134529561, ISBN-13: 9780134549897, 9780134529561, 5th ed.: 2013, ISBN-10: 0132774208, ISBN-13: 9780132774208. **2) Windows laptop or desktop for circuit design and verification (prelabs).**

All homeworks, prelab assignments and instructions will be posted on Blackboard. Individual prelab reports are due by midnight before the lab session.

Grading: Lab reports (40 pts), Homeworks (10 pts), Test 1 (10 pts), Test 2 (15 pts), Final exam (25 pts).
Final grades are determined as follows: A: > 92, A-: 91-85, B+: 84-78, B: 77-71: B-: 70-64, C+: 63-57, C: 56-50 pts.
Passing the course with grades in A-C range requires: 1) submission of 11 individual prelab reports (simulations) to the instructor; 2) best effort in 11 lab experiments and submission of the all final lab reports; 3) demonstration of the ability to design finite state machines on the final exam.

Topical outline:

1. Binary numbers and codes: 5 %
2. Boolean algebra, logic transformation and minimization: 20 %
3. Arithmetic circuits, decoders, multiplexers, latches and flip-flops: 25 %
4. Analysis and design of sequential circuits: 30 %
5. Memory and programmable logic: 20 %

Additional reading:

1. F. Vahid, Digital Design with RTL Design, VHDL, and Verilog, 2nd ed, 2010, ISBN-13: 978-0470531082, ISBN-10: 0470531088
2. D.M. Harris, S.L. Harris, Digital Design and Computer Architecture, 2nd ed., 2012, ISBN-13: 978-0123944245, ISBN-10: 0123944244
3. J. Wakerly, Digital Design: principles and practices, with Verilog, 5th ed., 2017, ISBN-13: 978-0134460093, ISBN-10: 013446009X

Tentative schedule

Wk	Mondays	Fridays	Topics	Labs	Pages 6 th ed.
1	Lecture 1 8/26	Lecture 2 8/30	Binary numbers, base conversion. Addition and subtraction, 2's complements.	**Lab is closed.** Installation of Active-HDL on a Windows PC.	1-37
2	No lecture 9/2	Lecture 3 9/6 HW 1	Logic operations and gates. Boolean algebra. Standard forms. Two-level implementations. Test signals, waveforms, critical path, racing, static glitches**.**	Prelab for Lab 1. Simulation. report is due by midnight before Lab 1 (1 point). **Lab is closed**	40-76
3	Lecture 4 9/9	Lecture 5 9/13 HW 2	Logic maps. Minimization. Form conversion. AOI and OAI implementations. Incompletely specified functions. Binary codes. Code converters	Lab 1 Board and logic analyzer. Propagation delays (2 points)	83-120
4	Lecture 6 9/16	Lecture 7 9/20 HW 3	Multiplexers, demultiplexers. Transmission gate. Cascading. Implementation of switching functions.	Lab 2 Two-level implementations (2 points).	175-189, 625-637
5	Lecture 8 9/23	Lecture 9 9/27 HW 4	Decoders, encoders. Implementation of switching functions. Adders. Inversion property. Subtractors. Overflow detection.	Lab 3 Design with multiplexers (3 points).	121--140
6	Lecture 10 9/30	Lecture 11 10/4 HW5	CMOS static, dynamic, PTL implementations. Introduction to Verilog HDL. Review.	Lab 4 Decoders (3 points).	156-170
7	Lecture 12 10/7	**Test 1 10/11**	Problem solving.	Lab 5 Encoder for flash ADC (3 points)	Ch. 1-4 review
8	No Lecture 10/14	Lecture 13 10/18	SR- and D—latches. Critical racing. Metastability. Setup time. CMOS Master–slave D- flip-flop. Preset and clear.	**Lab is closed**	246-260
9	Lecture 14 10/21	Lecture 15 10/25 HW 6	Analysis and design of synchronous Finite State Machines. Mealy and Moore outputs. Output glitches and delays	Lab 6 Adders (3 points)	261-316, 326-330
10	Lecture 16 10/28	Lecture 17 11/1 HW 7	Max clock frequency. Counters. Registers. Register-based counters. Hang-up states. State decoding.	Lab 7 State elements: latches and flip-flops (4 points)	352-365
11	Lecture 18 11/4	Lecture 19 11/ HW 8	Register Transfer Level design. Datapath and controller. Algorithmic State Machine chart. Review	Lab 8 Sequence generator (4 points)	430-540
12	Lecture 20 11/11	Lecture 21 11/15 HW9	Serial Peripheral Interface. Inter-Integrated Circuit interface. Field Programmable Gate Arrays. Review	Lab 9 Counter (5 points)	Ch. 4-8 review
13	Lecture 22 11/18	**Test 2 11/22**	Problem solving.	Lab 10 Datapath and controller for SPI ADC (5 points)	300-305
14	Lecture 23 11/25	No Lecture 11/29	Data scrambling. Cycling Redundancy Check. State assignments. State reduction, implication chart, partitioning.	**Lab is closed**	378-424
15	Lecture 24 12/2	Lecture 25 12/6 HW10	Flash, static, dynamic memories. Refreshing, bandwidth, latency. Review.	Lab 11 FPGA datapath and controller for SPI DAC (5 points)	assigned reading
16	Lecture 26 12/9		Problem solving, Lab 11 report is due in class	**Lab is closed**	

Final exam

If you have a physical, psychological, medical or learning disability that may impact your course work, please contact Disability Support Services, ECC (Educational Communications Center) Building, room128, (631) 6326748. They will determine with you what accommodations, if any, are necessary and appropriate. All information and documentation is confidential. Each student must pursue his or her academic goals honestly and be personally accountable for all submitted work. Representing another person's work as your own is always wrong. Faculty are required to report any suspected instances of academic dishonesty to the Academic Judiciary. For more comprehensive information on academic integrity, including categories of academic dishonesty, please refer to the academic judiciary website at http://www.stonybrook.edu/uaa/academicjudiciary/ Stony Brook University expects students to respect the rights, privileges, and property of other people. Faculty are required to report to the Office of Judicial Affairs any disruptive behavior that interrupts their ability to teach, compromises the safety of the learning environment, or inhibits students' ability to learn.